AD-772 526

# CARRIER AND BIT SYNCHRONIZATION METHODS FOR PSK SYSTEMS

Don J. Torrieri

Naval Research Laboratory
Washington, D. C.

December 1973

UNCLASSIFIED
Security Classification

AD 772526

**DOCUMENT CONTROL DATA - R & D**

*Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)*

1 ORIGINATING ACTIVITY (Corporate author)
Naval Research Laboratory
Washington, D.C. 20375

2a. REPORT SECURITY CLASSIFICATION
UNCLASSIFIED

2b. GROUP
---

3 REPORT TITLE
CARRIER AND BIT SYNCHRONIZATION METHODS FOR PSK SYSTEMS

4 DESCRIPTIVE NOTES (Type of report and inclusive dates)
Tutorial introduction to the synchronization problem.

5 AUTHOR(S) (First name, middle initial, last name)
Don J. Torrieri

| 6 REPORT DATE | 7a. TOTAL NO. OF PAGES | 7b. NO. OF REFS |
|---|---|---|
| December 1973 | 26 | 0 |

| 8a. CONTRACT OR GRANT NO | 9a. ORIGINATOR'S REPORT NUMBER(S) |
|---|---|
| NRL Problem 79R06-55 | NRL Memorandum Report 2689 |
| b. PROJECT NO<br>ND02.01.D | |
| c. | 9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report) |
| d. | |

10 DISTRIBUTION STATEMENT
Approved for public release; distribution unlimited.

| 11 SUPPLEMENTARY NOTES | 12 SPONSORING MILITARY ACTIVITY |
|---|---|
| | Department of the Navy<br>Naval Air Systems Command<br>Washington, D.C. 20361 |

13 ABSTRACT

This report provides an overview of the basic carrier and bit synchronization methods available for PSK systems. The report is intended also to serve as a tutorial introduction to the synchronization problem. It is written for the engineer familiar with the operation of a linear phase-locked loop.

DD FORM 1 NOV 65 1473 (PAGE 1)
S/N 0101-807-6801

UNCLASSIFIED
Security Classification

| 14 KEY WORDS | LINK A | | LINK B | | LINK C | |
|---|---|---|---|---|---|---|
| | ROLE | WT | ROLE | WT | ROLE | WT |
| Synchronization | | | | | | |
| Carrier synchronization | | | | | | |
| Bit Synchronization | | | | | | |
| Coherent demodulation reference | | | | | | |
| Phase shift key ( PSK) | | | | | | |
| Phase-locked loop | | | | | | |
| Squaring loop | | | | | | |
| Costas loop | | | | | | |
| Decision-directed loop | | | | | | |

## ABSTRACT

This report provides an overview of the basic carrier and bit synchronization methods available for PSK systems. The report is intended also to serve as a tutorial introduction to the synchronization problem. It is written for the engineer familiar with the operation of a linear phase-locked loop.

# Carrier and Bit Synchronization Methods for PSK Systems

## THE SYNCHRONIZATION PROBLEM

To understand the synchronization requirements of a coherent PSK (Phase-Shift Keying) system, it is easiest to first examine the ideal receiver for the case where both carrier sync and bit sync signals are available. The transmitted signals are assumed to be $+\sqrt{2}\sin\omega t$ for the binary ONE and $-\sqrt{2}\sin\omega t$ for the binary ZERO. The ideal receiver and the associated waveforms are shown in Figure 1. The noisy received signal is multiplied by the coherent (in phase) carrier reference to obtain a signal proportional to

$$\pm \sin^2 \omega t = \pm \frac{1}{2} (1 - \cos 2\omega t)$$

The double frequency term is effectively removed by the matched filter, which is an integrate and dump circuit. Bit synchronization is required in the matched filter to discharge the integrator properly; it is also required to sample at the proper time. The output of the sample and hold circuit is the data sequence.

The objective of synchronization is to obtain the necessary coherent demodulation reference (carrier sync) and bit sync with maximum efficiency. Inaccurate carrier sync results in a reduced effective signal to noise ratio at the input to the matched filter. Inaccurate bit sync results in either premature or late sampling, which increases the bit error probability.

One of the most important design criteria for a synchronization system is to use as little power as possible to achieve synchronization. In this way the maximum amount of energy shall be available for the transmission of the data. Thus, the transmission of synchronization information via a separate carrier, which squanders bandwidth as well as power, cannot be considered a satisfactory method.

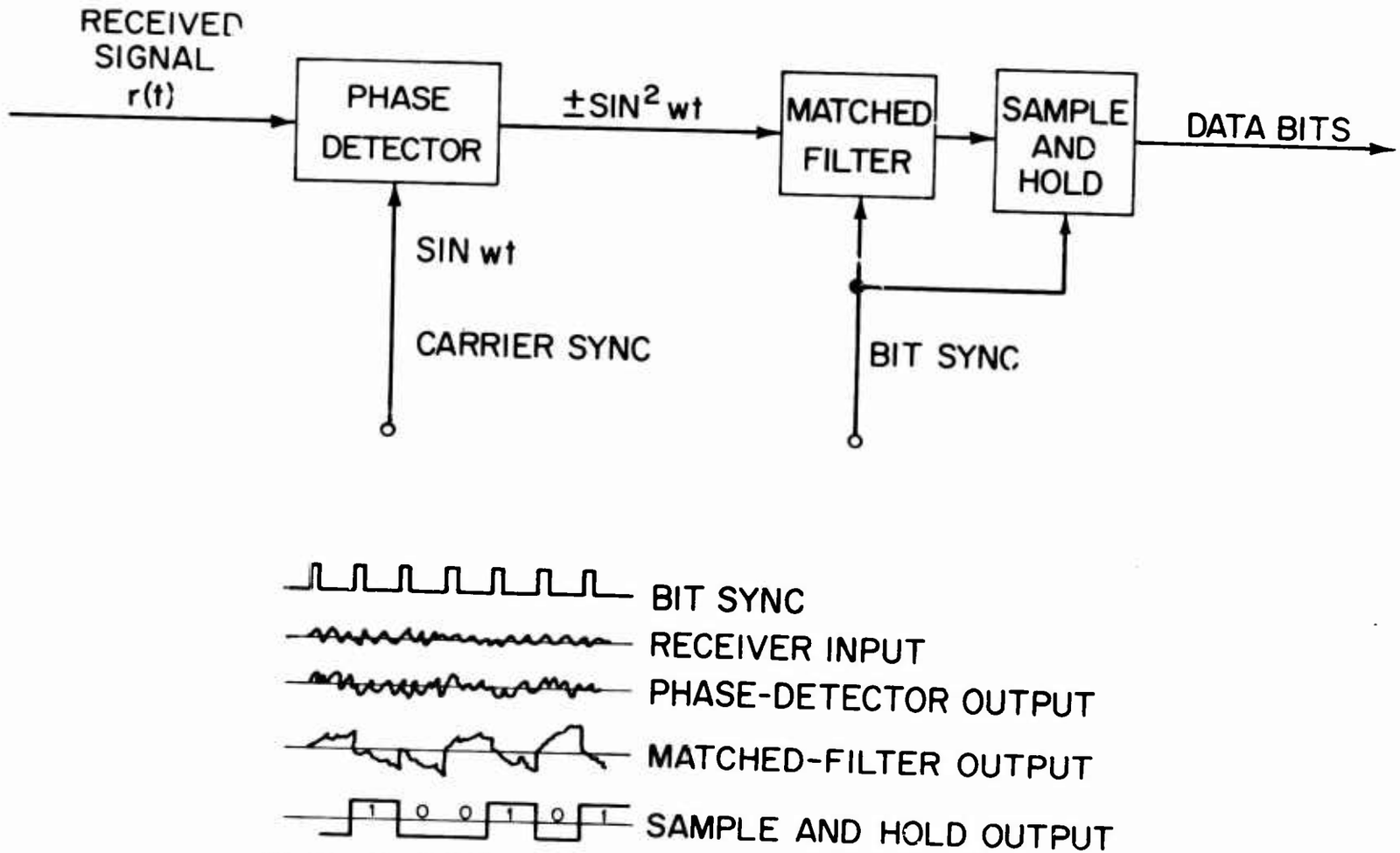


Fig. 1 - Ideal PSK receiver when synchronization signals are available

Often, a third level of synchronization is required to separate the detected data bits into words. There are three basic methods of word synchronization:

1. Transmission of frame synchronization patterns, which indicate the beginning of a group of words. Once these patterns are recognized, word synchronization is easily obtained from bit sync through a frequency division.

2. Separate channel transmission. If word sync is established by this means, bit sync may be easily obtained by a frequency multiplication. If frame sync is established by this means, bit sync information is needed to obtain word sync by frequency division.

3. Coding of the data transmission. Usually, pseudo-noise sequences are superimposed on the data to convey word or frame sync information. This method is the most efficient from the viewpoint of power utilization. The details of this method are complex and beyond the scope of this report.

## CARRIER SYNCHRONIZATION

If sufficient energy were available at the carrier frequency, the carrier synchronization could be achieved by means of a phase-locked loop, as shown in Figure 2. The noisy data bits which emerge from the output filter are sent to the bit synchronizer, which will be described in the next section.

Unfortunately, if the PSK signals are randomly modulated, the energy available at the carrier frequency is not sufficient for the satisfactory performance of the simple system of Figure 2. It is necessary to perform some nonlinear operation on the received signal to ensure that the carrier frequency or some harmonic of it will have enough energy to make phase-lock attainable. If white Gaussian noise is present at the input of the system of Figure 2, the variance of the phase error of the voltage controlled oscillator (VCO) is given by

$$\sigma^2 = \frac{NB}{S} \tag{1}$$

where N is the noise power spectral density, S is the mean signal power, and B is the loop noise bandwidth. This equation is derived by using a linear model for the phase-locked loop.

The most commonly used nonlinear system for carrier synchronization is the squaring loop illustrated in Figure 3. The bandpass filter should be wide enough to pass the signal with negligible distortion, but otherwise as narrow as possible. After passing through the square law device, the signal becomes

$$\left(\pm\sqrt{2}\sin\omega t\right)^2 = 1 - \cos 2\omega t$$

The DC term is suppressed by the loop filter and phase-lock is achieved with the double frequency term. Thus, in the absence of any phase error, a coherent reference is provided by the VCO, which has the output proportional to

$$-\cos(\omega t + \pi/2) = \cos(\omega t + \pi/2 + \pi) = \sin\omega t$$

Demodulated data is obtained by multiplication of the coherent reference and the bandpass filter output.

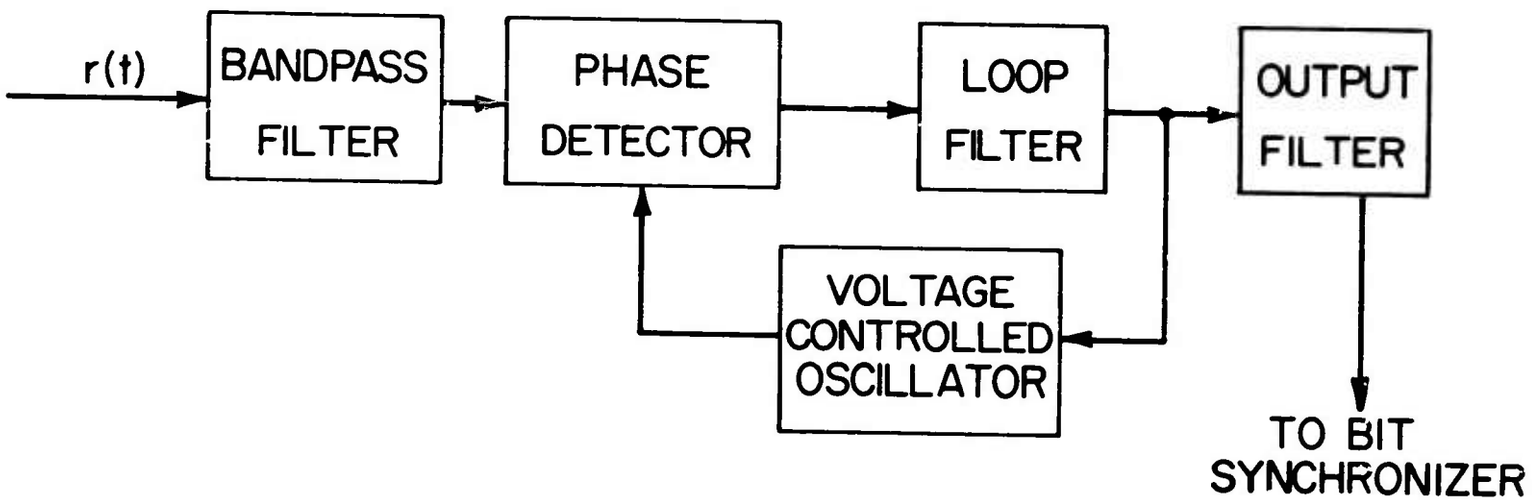


Fig. 2 - Phase-locked loop for carrier synchronization

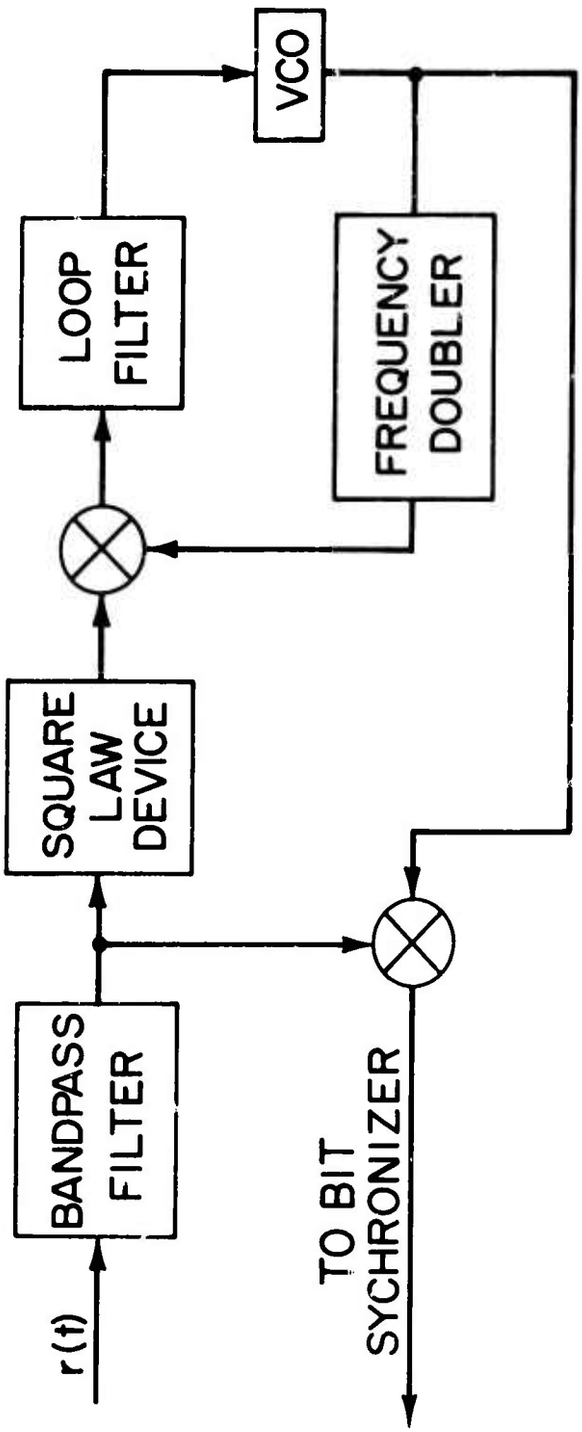


Fig. 3 – Squaring loop

The variance of the phase error of the VCO is given by

$$\sigma^2 = \frac{NB}{S}\left(1 + \frac{NW}{2S}\right) \qquad (2)$$

where W is the bandwidth of the bandpass filter. This equation shows the increase in variance due to the square-law nonlinearity.

Another nonlinear system, called the Costas loop, is illustrated in Figure 4. Its phase error variance is also given by equation (2), where W is now interpreted as the bandwidth of both bandpass filters.

To understand the Costas loop, it is easiest to consider its noise-free operation. When the Costas loop is in lock and the input signal is $s(t) = \pm \sin \omega t$, the VCO output is $\cos(\omega t - \phi)$ where $\phi$ is the phase estimation error. The negative 90 degree phase shifter produces an output of $\sin(\omega t - \phi)$. With the bandpass filters eliminating the double frequency terms, it follows that we have the following approximate relations:

$$Z_1(t) \sim \pm \sin \phi$$

$$Z_2(t) \sim \pm \cos \phi$$

where the symbol $\sim$ denotes proportionality. Thus, the input to the loop filter is proportional to

$$\sin \phi \cos \phi = \frac{1}{2} \sin 2\phi \simeq \phi$$

where the last relation holds for small $\phi$. This equation indicates that the VCO input is proportional to the phase error and is unaffected by the modulation. Thus, phase-lock will occur in the Costas loop. A more detailed calculation yields equation (2).

A slight modification of the Costas loop, called the modulation reconstruction loop, may be used for more rapid carrier acquisition. The alteration consists of placing a limiter between the signal $Z_2(t)$ and the multiplier feeding the loop filter.

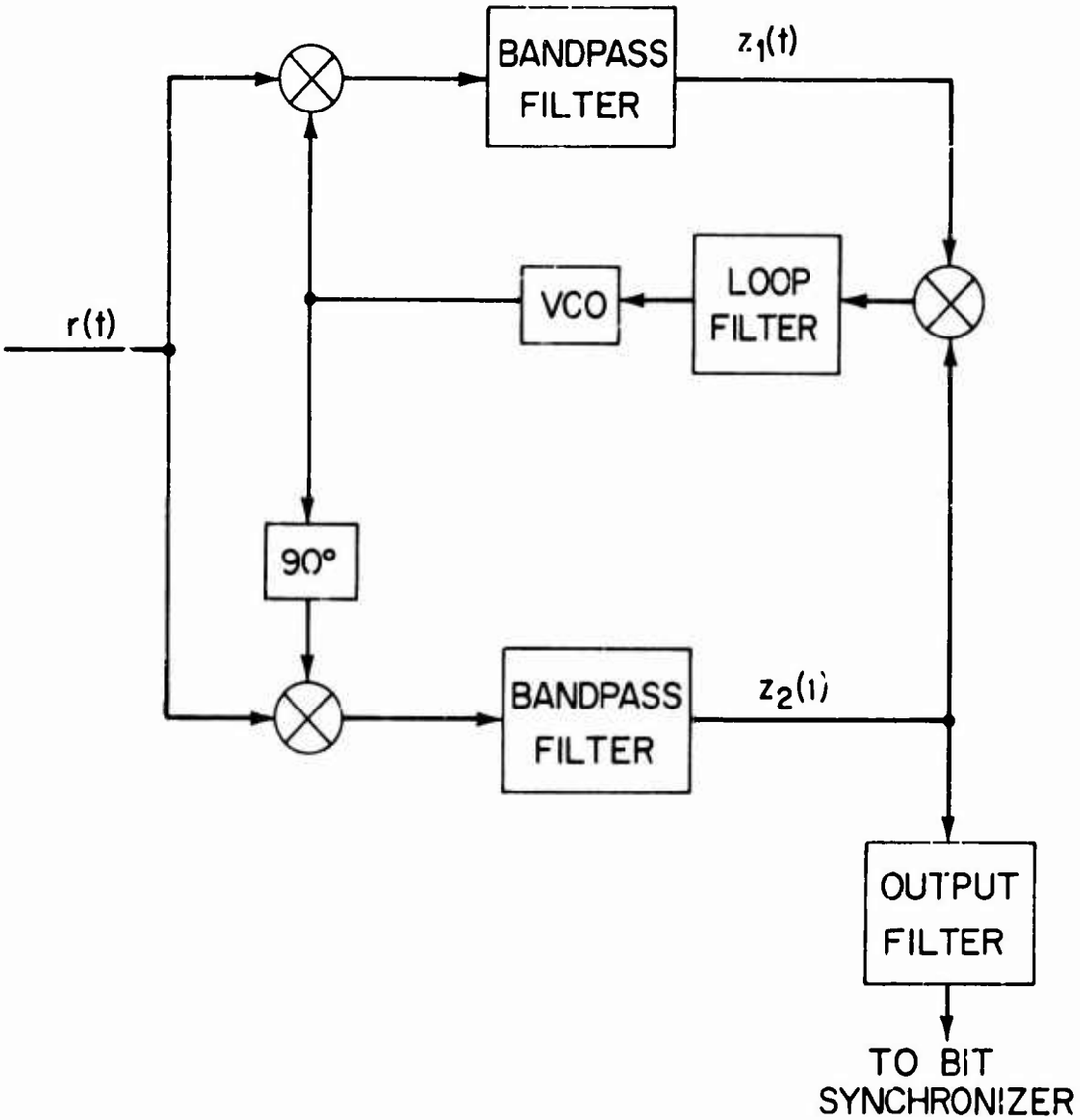


Fig. 4 - Costas loop

In all of the above systems, it has been assumed that bit synchronization is not available. However, if bit synchronization is somehow obtained (possibly from a separate channel), the Costas loop may be modified for more efficient operation. The resulting system, called the decision-directed loop, is shown in Figure 5, where the delay T is equal to the time duration of the data bits. The waveform Z(t) is the final demodulated data sequence.

Two variations of the decision-directed loop are worthy of mention. In one variation, the delay device is replaced by a matched filter-sample and hold configuration identical to that in the lower branch of Figure 5. In the second variation, the multiplier feeding the loop filter is eliminated. Instead, the data bits are used to shift by $\pm$ 180 degrees the VCO output.

It should be noted that carrier synchronization is possible in principle without a phase-locked loop if the carrier possesses sufficient energy. Because a loop is capable of tracking the signal frequency, its bandwidth $B_L$ can be much narrower than the dynamic frequency range $\Delta f$ of the received signal. Nevertheless, the received signal could be filtered with a passive filter having bandwidth $B \approx \Delta f$. It can be shown that to obtain the same accuracy with the filter as is attainable with the phase-locked loop, the signal power must be increased by a factor of $B/B_L$.

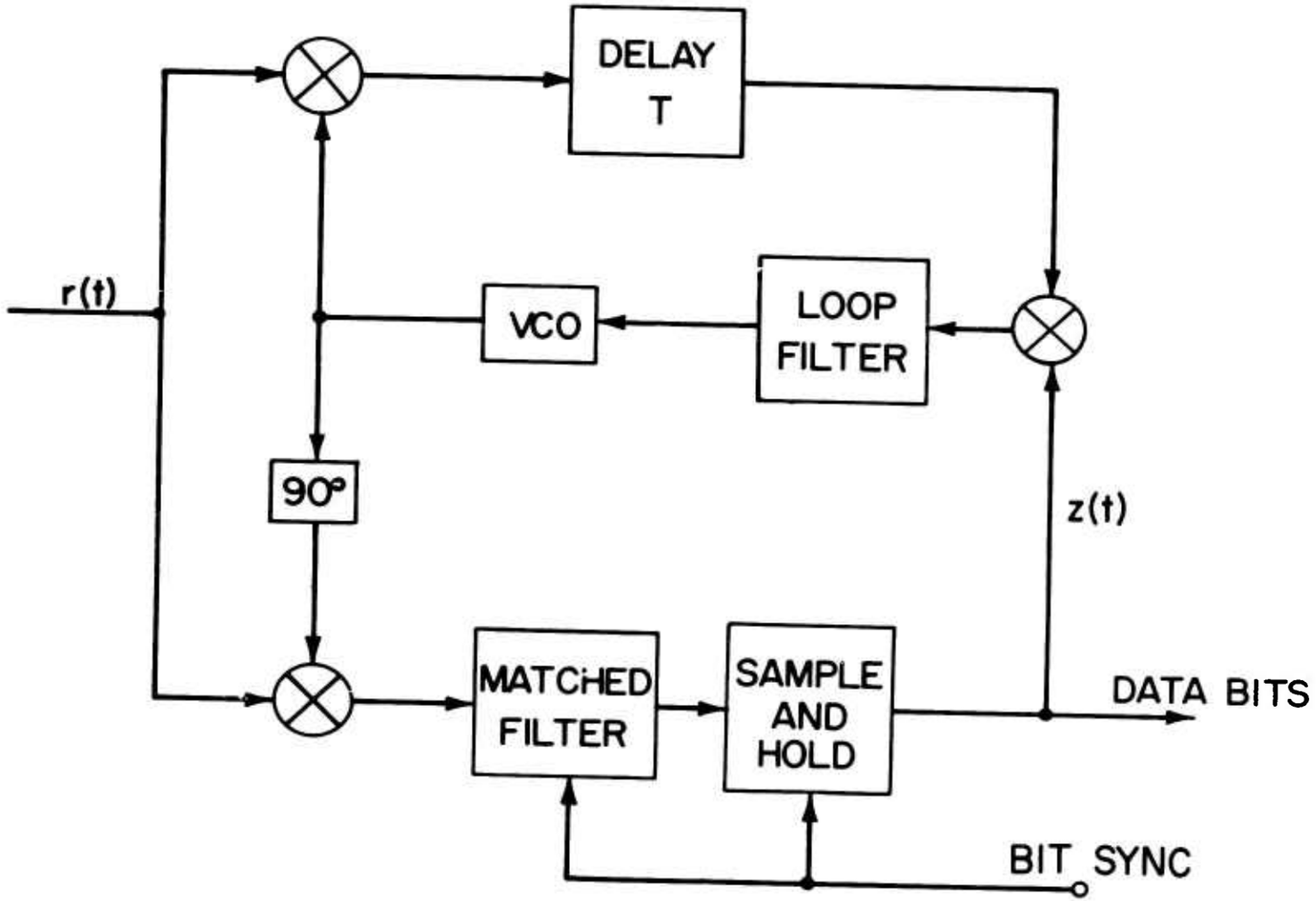


Fig. 5 - Decision-directed loop

## BIT SYNCHRONIZATION

The noisy, filtered data bits emerging from the carrier synchronization system must be detected and processed. To this effect it is necessary to have bit sync pulses, as indicated in Figure 1. Usually the bit sync pulses are derived from a clock that is coherent with the bit stream.

One method of obtaining a coherent clock is to transmit it via a separate channel. Not only does this increase the system complexity, it often presents interchannel interference problems which may degrade the system performance. Second, the power relegated to the synchronization channels represents power which could have been used to transmit data were some other means of synchronization available. For these reasons, it is preferable to obtain the clock directly from the data bits. Then all of the available power is used simultaneously for synchronization and communication.

Before proceeding with the discussion of bit synchronizers, it is necessary to examine the synchronization properties of the waveforms used in digital pulse signaling. Four common waveforms, illustrated in Figure 6, are return-to-zero (RZ), non-return-to-zero (NRZ), split-phase or Manchester, and Miller. As seen in Figure 6, the RZ waveform is a ternary code in which a logical ONE is represented by a half-symbol wide pulse of one polarity and a logical ZERO is represented by a half-symbol wide pulse of the opposite polarity. There are two types of NRZ formats. In NRZ-Level, a ONE is represented by one level and a ZERO by the other level. Differential encoding of the NRZ format results in the NRZ-Mark or NRZ-Space waveform. In NRZ-Mark, a ONE is represented by a level change and a ZERO by no change in level. In NRZ-Space, a ONE is represented by no level change and a ZERO by a change. The Manchester format results when NRZ-Level is multiplied by a clock having a frequency equal to the bit rate. Differentially encoded Manchester waveforms result when NRZ-Mark or NRZ-Space is multiplied by the clock. In the Miller format, a ONE is represented by a level change at the symbol period midpoint. A ZERO is represented by no change unless it is followed by another ZERO, in which case a transition is placed at the end of the period of the first ZERO.

The RZ, NRZ-Level, and Manchester waveforms produce an inherent 180 degree phase ambiguity at the carrier tracking loop output. In other words, the demodulated waveform emerging from the carrier synchronization system may be either the true message or its inverse. To eliminate the phase ambiguity problem, a small carrier component may

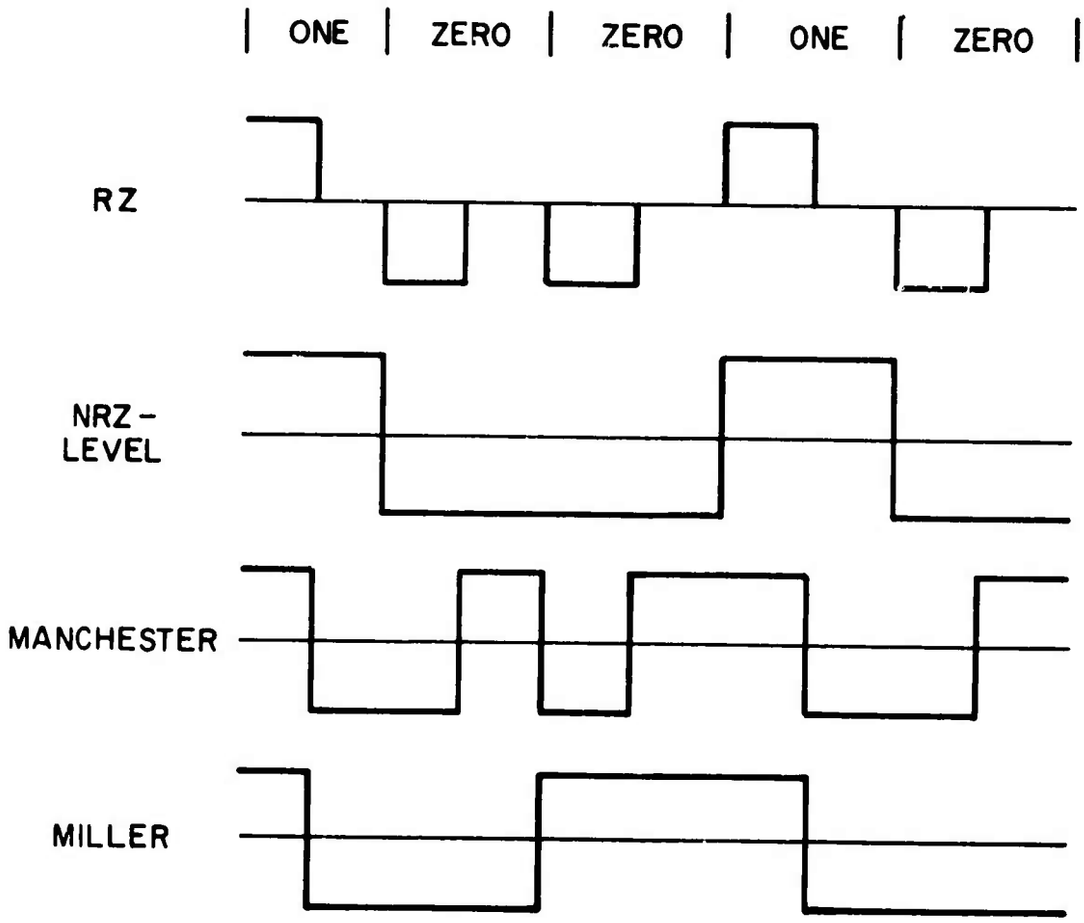


Fig. 6 - Some digital waveforms

be transmitted, the frame synchronization bits may be used, or the error control bits of the data stream may be employed. The Miller and the differentially encoded waveforms do not result in any phase ambiguity. This fact is one of the most attractive features of the latter formats.

All of these waveforms contain little energy at frequencies equal to the bit rate or one of its harmonics. Thus, it is impossible to recover the clock merely by application of the demodulated waveform to a phase-locked loop.

The key to bit synchronization is to locate the data transitions. An example of this method of timing recovery is shown in Figure 7. Figure 8 depicts the operation when a split-phase waveform is employed. Here differentiation marks the locations of the data transitions. The full-wave rectifier insures that pulses occur at least once very bit period. The output of the rectifier passes through a bandpass filter centered at the bit frequency, and the output signal is hard-limited to produce a clock signal nominally centered at the bit frequency. Unfortunately, the original noise appears in the form of jitter in the zero crossings; however, if the noise is not severe, the phase-locked loop is capable of tracking the jittered clock and producing a bit clock.

Clearly, we could obtain a clock from the other waveforms by using the same system of Figure 7. In the case of NRZ, the full-wave rectifier would have fewer output pulses. In the case of RZ, there would be two output pulses per bit period. Thus, most of the energy would be in the second harmonic of the bit rate and a half-wave rectifier might be more efficient.

The NRZ format does not guarantee level transitions at the bit rate. If successive data bits tend to be equal, the number of bit transitions are few, and the simple system of Figure 7 will not work properly. The Manchester and RZ schemes assure level transitions at the center of the bit period. Thus, these two waveforms tend to make the bit synchronizer performance virtually independent of the data statistics. Miller encoding provides enough transitions for effective bit synchronization. The dependence of bit synchronizer performance upon the stochastic properties of the data is weak and usually negligible.

One issue remains to be discussed--the processing of the clock signal to obtain the bit sync pulses shown in Figure 1. Looking at Figure 8, it is seen that the clock is 90 degrees out of phase with the limiter output. After

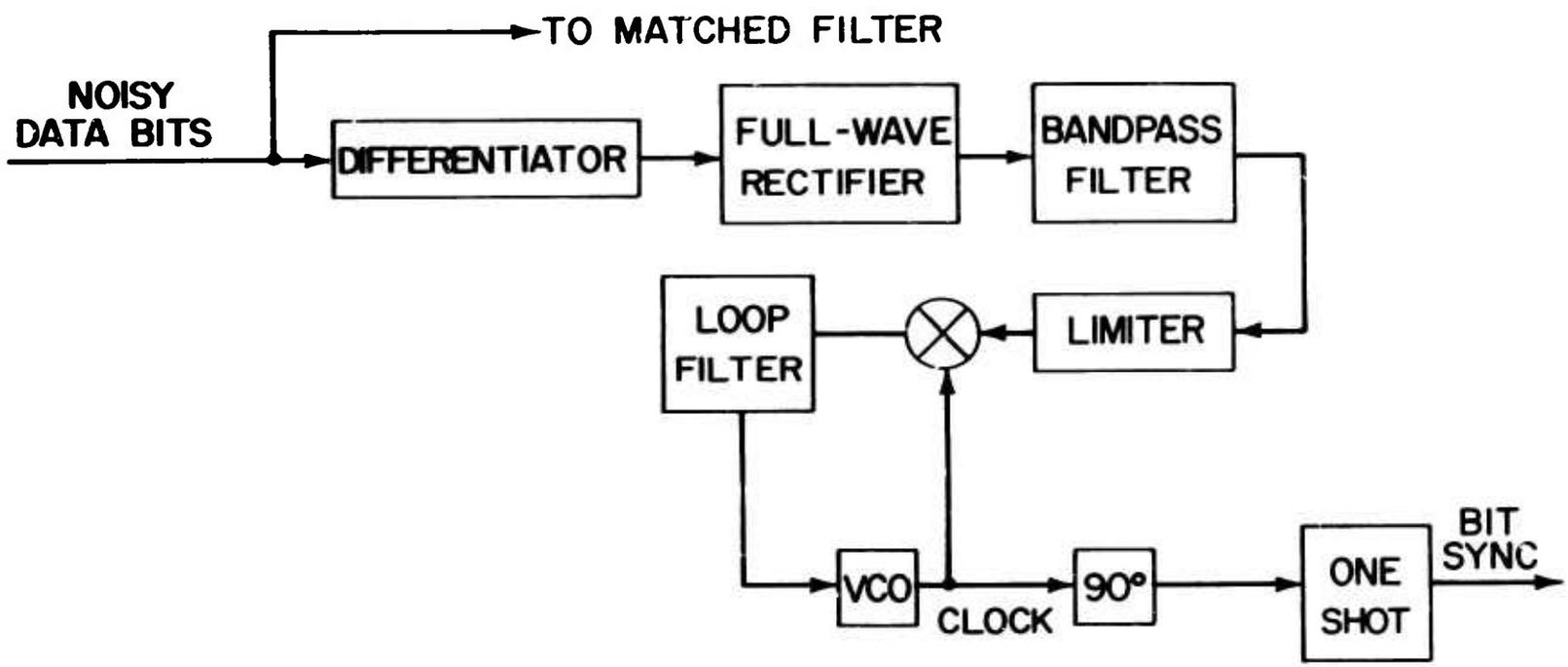


Fig. 7 – A bit synchronizer

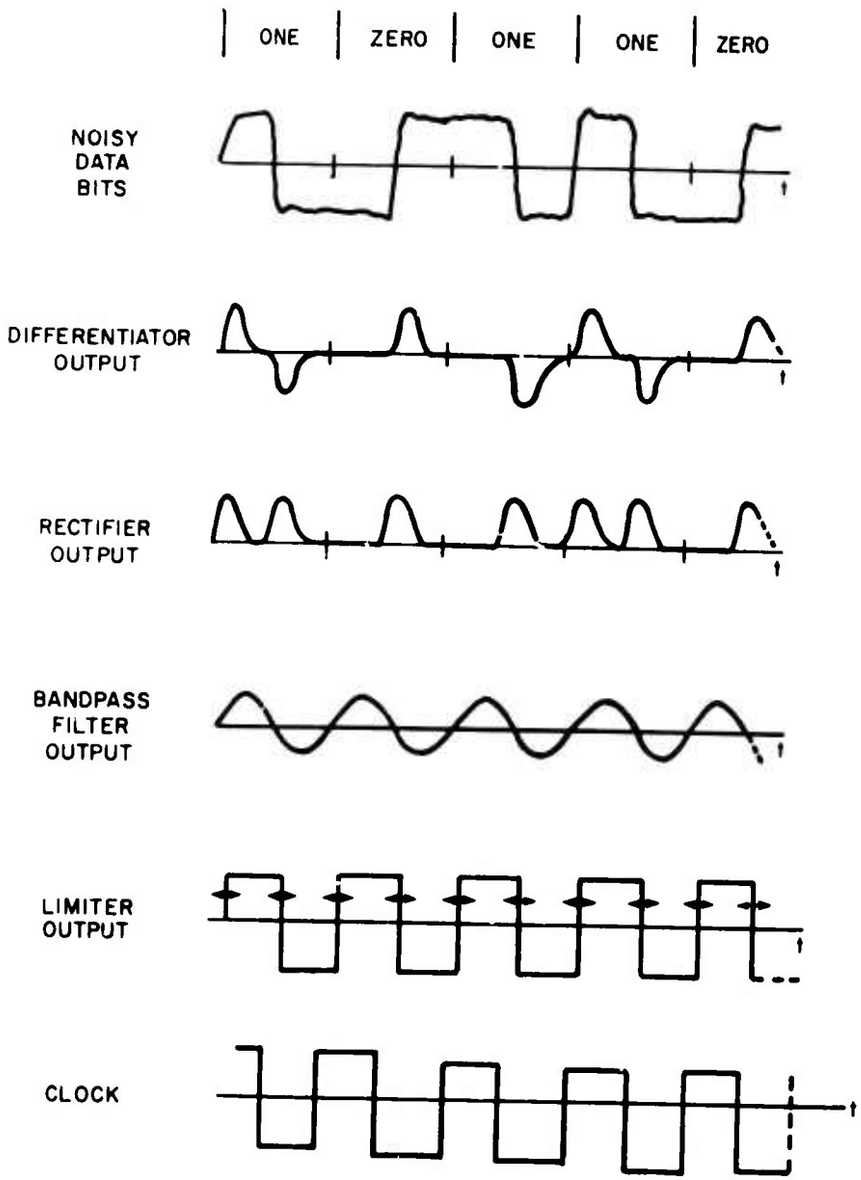


Fig. 8 - Clock Generation from a split-phase waveform

a negative 90 degree phase shift the positive-going edges of the clock signal are aligned with the bit boundaries. Thus, we can feed the clock into a monostable multivibrator (one-shot) set to respond to positive-going transitions. The output will be the bit sync pulses.

Other efficient bit synchronizers exist, but they lack the intuitive appeal of the system of Figure 7. These bit synchronizers, notably the early-late gate and the data transition tracking loop (DTTL), are usually motivated by the maximum a posteriori estimation of the symbol epoch. The DTTL was used as a bit synchronizer in the high-rate telemetry receiver of the Mariner Mars 1969 mission. Details of the operation of the DTTL and the early-late gate are too complicated to be considered in this introductory report. The interested reader should consult the book by Lindsey and Simon (1).

The synchronization properties of the digital waveforms have been investigated. However, the reader should be aware that there are other characteristics, not necessarily crucial to synchronization, which must be carefully considered before choosing a data format. Some of these characteristics are:

1. Bit error rate. The RZ format, which involves the transmission of less energy per bit, is inferior to NRZ in this respect.

2. Low DC spectral density. This characteristic is important in achieving a high packing density on magnetic tapes. The Manchester format has no DC component. The Miller format has a low DC spectral density. The others have considerable low frequency energy.

3. Bandwidth. The Miller and NRZ waveforms require about half the bandwidth needed by Manchester coding and about one fourth that needed by RZ.

## THE COHERENT PSK RECEIVER

There are several ways of combining the carrier and bit synchronization methods discussed to produce a complete coherent PSK receiver. The most obvious approach is to process the received waveform sequentially, as indicated schematically in Figure 9. A receiving system employing feedback is illustrated in Figure 10, where the estimated data bits are taken from the input to the matched filter of the decision-directed loop shown in Figure 5.

The simultaneous gereration of a coherent reference and a bit sync is possible with only a slight amount of additional effort. The method involves modulating the transmitted PSK signal with the bit synchronization information. Thus, we transmit and receive a signal proportional to

$$\pm \sin \frac{\pi t}{T} \sin \omega t$$

where T is the bit period and $\omega$ is the carrier frequency. The received signal passes through a square law device, as seen in Figure 11. Ignoring the noise and constant amplitude factors, the output of the device is

$$1 - \cos \frac{2\pi t}{T} - \cos 2\omega t + \frac{1}{2} \cos\left(2\omega - \frac{2\pi}{T}\right)t + \frac{1}{2} \cos\left(2\omega + \frac{2\pi}{T}\right)t$$

which has periodic components at double the carrier frequency and double the bit rate. The carrier double frequency is tracked by a phase-locked loop. The VCO output is proportional to $\sqrt{2} \sin(\omega t + \Phi)$, where $\Phi$ is the phase estimation error. The product of this output and the received signal, is equal to

$$\pm \sqrt{2} \sin \frac{\pi t}{T} \cos \Phi$$

assuming that the high frequency terms are eliminated. Another phase-locked loop tracks the component with a frequency of double the bit rate. If the modulating signal $\sin \frac{\pi t}{T}$ is originally obtained from the same reference as the carrier by dividing the frequency by a factor K, the

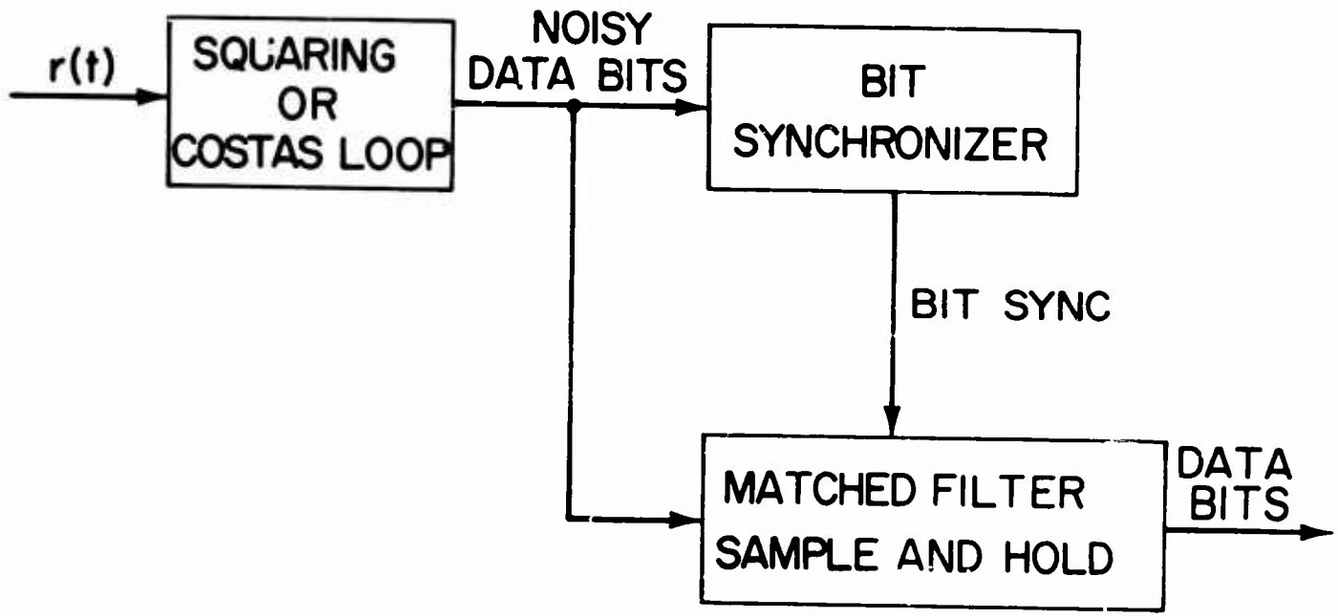


Fig. 9 - A coherent PSK receiving system with sequential synchronization

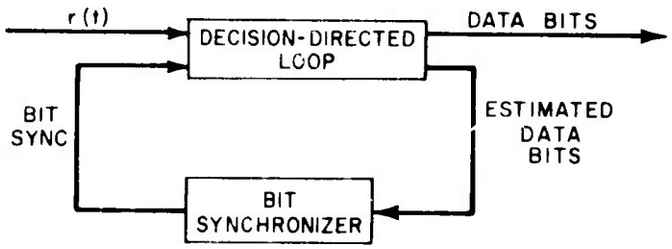


Fig. 10 - A coherent PSK receiving system with feedback synchronization

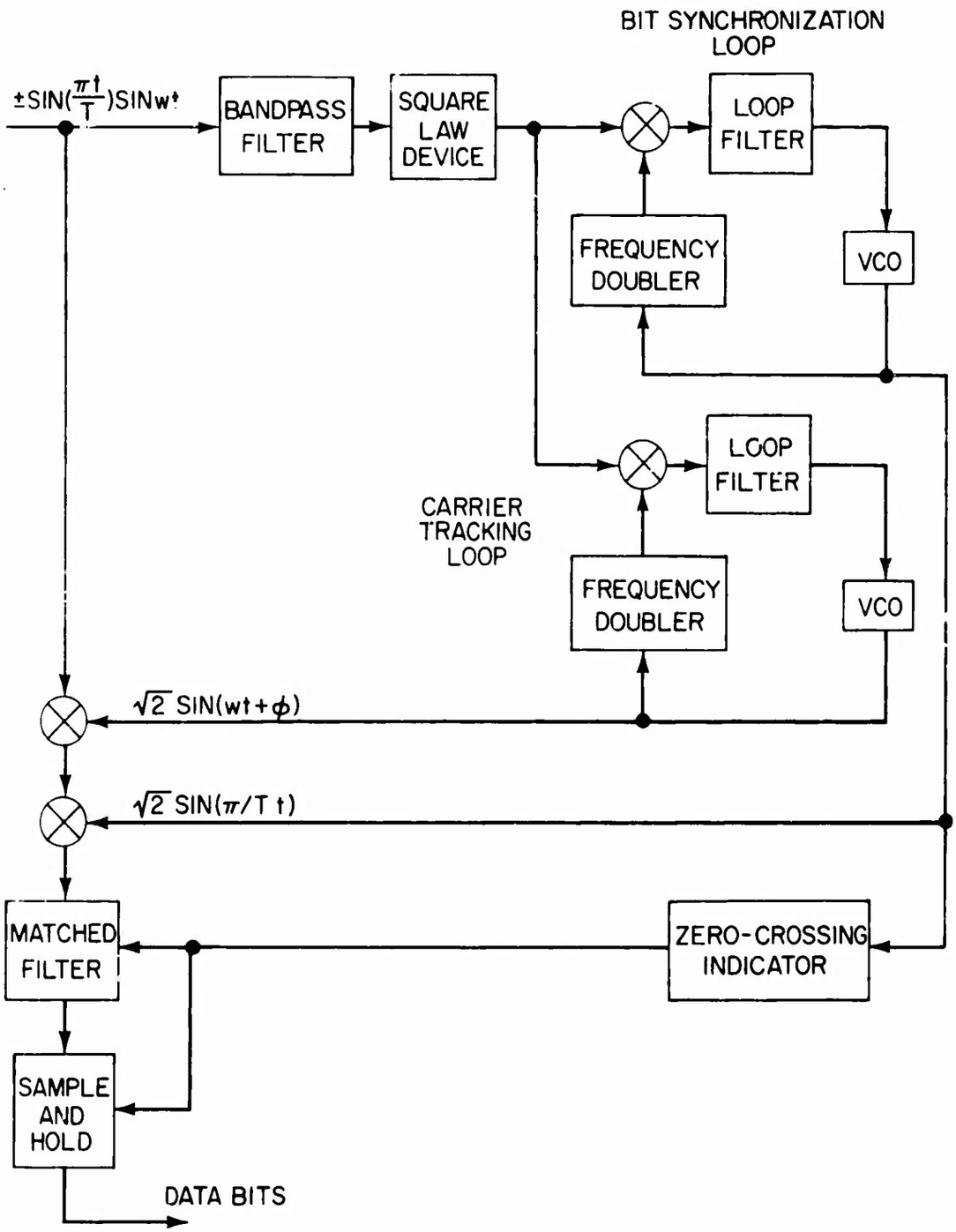


Fig. 11 – A coherent PSK receiving system with simultaneous carrier and bit synchronization

phase uncertainty of the modulation is 1/K the uncertainty of the carrier. Therefore, the bit synchronization loop bandwidth need be only 1/K the carrier tracking loop bandwidth. Consequently, the phase estimation error of the bit synchronization loop is negligible when K is large. The VCO output is approximately $\sqrt{2}\sin\frac{\pi}{T}t$. This signal is passed through a zero-crossing indicator which produces the bit sync pulses. The same signal is applied to a multiplier, the output of which is proportional to

$$\pm\left(1 - \cos\frac{2\pi t}{T}\right)\cos\phi$$

if the high frequency terms are ignored (the latter are effectively eliminated by the matched filter if $\omega T >> 1$). The matched filter output at the end of a bit period is proportional to

$$\pm\int_0^T \left(1 - \cos\frac{2\pi t}{T}\right)\cos\phi\, dt = \pm T\cos\phi$$

It is seen that the effective signal power applied to the matched filter is reduced by a factor $\cos^2\phi$ due to the phase estimation error. A more careful analysis shows that the phase error variance for the system is once again given by equation (2).

SUPPLEMENTARY READING

1. W. C. Lindsey and M. K. Simon, Telecommunication System Engineering, Prentice-Hall, New Jersey, 1973.

2. W. C. Lindsey, Synchronization Systems in Communication and Control, Prentice-Hall, New Jersey, 1972.

3. J. J. Stiffler, Theory of Synchronous Communications, Prentice-Hall, New Jersey, 1971.

4. A. J. Viterbi, Principles of Coherent Communication, McGraw-Hill, New York, 1966.